Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**DIE FUNCTIONS:**

1. **IN 1A**
2. **IN 1B**
3. **OUT 1**
4. **IN 2A**
5. **IN 2B**
6. **OUT 2**
7. **GND**
8. **OUT 3**
9. **IN 3A**
10. **IN 3B**
11. **OUT 4**
12. **IN 4A**
13. **IN 4B**
14. **VCC**

**.030”**

**.036”**

**5 4 3 2**

**6**

**7**

**8**

**1**

**14**

**13**

**9 10 11 12**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: LS00**

**APPROVED BY: DK DIE SIZE .030” X .036” DATE: 8/30/21**

**MFG: MOTOROLA THICKNESS .015” P/N: 54LS00**

**DG 10.1.2**

#### Rev B, 7/1